PEX7-COP

PRELIMINARY rev 0.96 02/09/18

Innovative Integration
a molex company

PCI Express Desktop/Server Coprocessor with Kintex-7 FPGA Computing Core and FMC I/O Site

FEATURES

- Desktop/Server 3/4 full-length FPGA Coprocessor Card
- FMC HPC I/O site (VITA 57) with x8 10.0 Gbps MGT lanes, 80 LVDS pairs (LA, HA, HB full support)
- FPGA Computing Core
    - Xilinx Kintex-7 K325 or K410
    - Single Bank 256Mb x 64 DDR3 (2048 MB total)
    - 256Mb BPI Configuration FLASH
- External clock input
- External trigger input supports multi-card synchronization and coordinated sampling
- 1 PPS Input
- 8 lane PCIe Express Gen 2 interface providing 4 GB/s burst and 3.2 GB/s sustained transfer rates
- On-board USB to JTAG programmer allows FPGA programming without external hardware
- 14-pin JTAG header with Xilinx compatible pinout
- < 15W typical power excluding FMC
- Temperature and power monitoring

APPLICATIONS

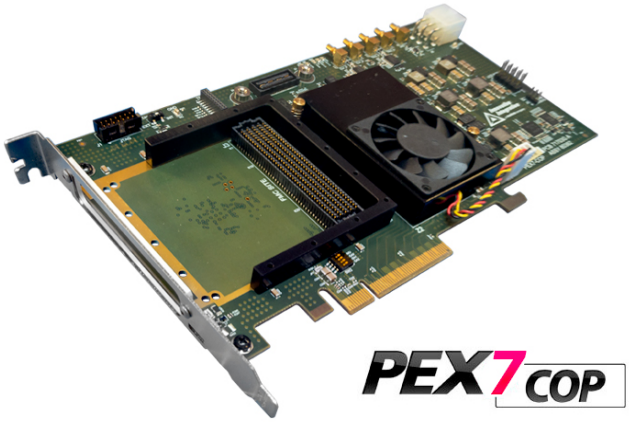
- FPGA co-processing and acceleration
- Wireless Receivers – LTE, WiMAX, SATCOM
- RADAR, Signal Intelligence
- Medical Imaging
- High Speed Data Recording and Playback
- IP development

SOFTWARE

- MATLAB/VHDL FrameWork Logic
- VxWorks/LinuxWindows Drivers
- Microsoft and Codegear C++ Host Tools
- Software required for the USB JTAG Programmer operation is available free of charge from Xilinx and Digilent

MATLAB XILINX

FMC



DESCRIPTION

The PEX7-COP is a flexible FPGA co-processor card that integrates a Kintex-7 FPGA computing core with an industry-standard FMC I/O module on a three-quarter-length PCI Express desktop or server card.

The FPGA computing core features the Xilinx Kintex-7 FPGA family and is offered in two densities, K325 or K410. The K410 FPGA provides over 2000 DSP MAC elements operating at up to 500 MHz. The FPGA core has a 2048 MB DDR3 DRAM bank attached.

For system communications, the PEX7-COP utilizes a PCI Express x8 Gen2 port capable of up to 3.2 GB/s sustained operation with 4 GB/s burst rate.

An FMC site, conforming to VITA 57 standard, provides configurable I/O for the PEX7-COP. The FMC site has full support for the high pin count connector (HPC), with 80 LVDS pairs and 8 high-speed lanes (TX/RX) at up to 10 Gbps per lane directly connected to the FPGA. The FMC site is readily adapted to application-specific custom modules.

The FPGA logic can be fully customized using the Frame Work Logic tool set. The toolset provides support for both MATLAB and RTL designs. The MATLAB BSP supports real-time hardware-in-the-loop development using the graphical, block diagram Simulink environment with Xilinx System Generator. IP cores for a range of signal processing cores for applications such as wireless, RADAR and SIGINT such as DDC, demodulation, and FFT are also available.

Software tools for host development include C++ libraries and drivers for Windows and Linux (including real-time variants). Application examples demonstrating the module features are provided.

PEX7-COP

This electronics assembly can be damaged by ESD. Innovative Integration recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

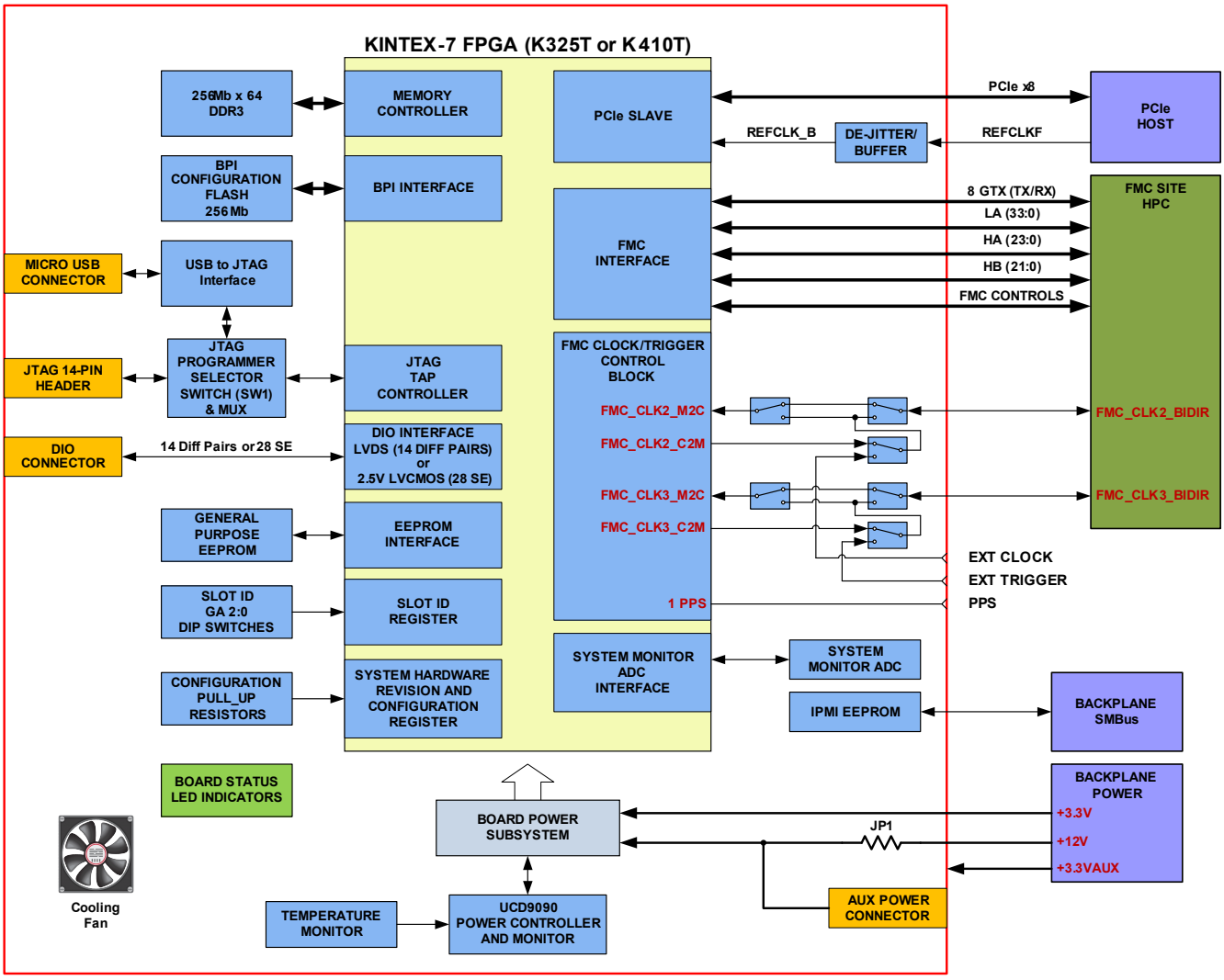
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

Product	Part Number	Description
PEX7-COP, K325T, -2 SPEED, IND. TEMP	80382-0-L0	PEX7-COP with XC7K325T-2FFG900I FPGA
PEX7-COP, K410T, -2 SPEED, IND. TEMP	80382-1-L0	PEX7-COP with XC7K410T-2FFG900I FPGA
Breakout Board, no cable	80350-5-L0	FMC Breakout Board, all SMA Connectors, no Cable
Breakout Board with 36” Cable	80350-1-L0	FMC Breakout Board, all SMA Connectors with 3 ft EQCD Ribbon Coaxial Cable
36” Cable Ribbon Coax Cable	67227	Cable Assembly, 3 ft EQCD Ribbon Coaxial Cable
PCIe Satellite DIO, PEX7-COP	80386-0-L0	Expansion DIO Board for DIO from FMC module on PEX7-COP
Cable Assy, Ribbon Coax, 2x20	672xx	Cable from PCIe Satellite DIO to PEX7-COP
PEX7-COP FrameWork Logic	550xx	PEX7-COP FrameWork Logic board support package for RTL and MATLAB. Includes technical support for one year. Check with sales for specific FMC support.
Software	57001	Malibu software installation DVD including drivers for Windows and Linux.

PEX7-COP

BLOCK DIAGRAM



PEX7-COP

Standard Features

Physicals	
Form Factor	PCI Express, ~ 3/4 Full Size card
Size	206.4 mm x 111.1 mm (8.125 in x 4.375)
Weight	~213g (7.5 oz), without FMC
Hazardous Materials	Lead-free and RoHS compliant

Power (PEX7-COP only, no FMC)	
Voltage	**Current**
3.3V (+/-5%)	1A Maximum. Supplied by the host computer
12V (+/-5%)	1.2A Maximum. Supplied by the host computer OR from the J8 Auxiliary Connector (jumper JP1 must be removed to avoid potential damage)
3.3VAUX (+/-5%)	50mA Maximum. Supplied by the host computer
Power Consumption	15W typical

FMC Power Available	
Voltage	**Current**
3.3V (+/-5%)	3A Maximum. Supplied by the host computer
12V (+/-5%)	2A Maximum. Supplied by the host computer OR from the J8 Auxiliary Connector (jumper JP1 must be removed to avoid potential damage)
Vadj (+/-5%; 2.5V standard)	4A Maximum. Generated on the PEX7-COP board
3.3VAUX (+/-5%)	20mA Maximum. Supplied by the host computer

Power and Thermal Control	
Temperature Monitor	Software with programmable alarms
Over-temp Monitor	Disables power supplies
Alerts	Temperature Warning, Temperature Failure, Power Faults
Alert Timestamping	5 ns resolution, 32-bit counter
Power Control	LPDDR3 deep sleep mode FMC power controls
Heat Sinking	Heat sink with fan, on FPGA

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FMC Site	
Specification	VITA 57 FMC, HPC
High Speed Pairs	8 lanes (Tx/Rx pair); 10 Gbps max rate
Signal Pairs	80 diff pairs total LA: 34 diff pairs (K7 FPGA) HA: 24 diff pairs (K7 FPGA) HB: 22 diff pairs (K7 FPGA)
I/O Standards	LA: all I/O standards available in an HR bank, with VCCO = VADJ voltage HA: all I/O standards available in an HR bank, with VCCO = VADJ voltage HB: all I/O standards available in an HR bank, with VCCO = VIO_B voltage Choice of I/O standards is also constrained by FPGA limitations on which standards can be used together in the same HR bank.

FPGA	
Device	Xilinx Kintex-7
Speed Grade	-2
Logic Cells	K325T: 326K K410T: 406K
Flip-Flops / Slices	K325T: 407K /50K K410T: 508K /63K
DSP48E1 elements / Total Block RAM	K325T: 840 / 16,020 Kb K410T: 1540 / 28,620 Kb
GTX Transceivers	16 available: 8 for PCIe, 8 for FMC High Speed Pairs Max 10.3125 Gb/s data rate is supported for speed grade -2
Configuration	JTAG or FLASH; In-system re-programmable

Memories	
DDR3 SDRAM	256Mb x 64 (2048MB) Clock rate 800 MHz (DDR3 1600)
BPI Configuration FLASH	Parallel NOR FLASH Memory 256Mb, Eight 32Mb partitions
General Purpose EEPROM	SPI FLASH, 128Mb
IPMI EEPROM /Temperature sensor	8 Kb EEPROM

Host Interface	
PCI Express	x8 Lanes Gen2 (-2 or -3 speed grade FPGA required; with -1 speed grade FPGA the PCIe speed is limited to Gen1) Supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates

Sample Clocks and Triggering	
External Clock*	Single-ended; AC-coupled; 0.3Vp-p min, 1.5Vp-p max; 50 Ohm Input Impedance
External Trigger*	Single-ended; DC-coupled; Vin low = 0V to 0.7V; Vin high = 1.7V to 2.5V; 500 Ohm Input Impedance
1 PPS	Single ended; DC-Coupled; Vin low = 0V to 0.6V; Vin high = 1.2V to 5.5V; 10 KOhm Input Impedance

Note: For other external clock and trigger input configuration options, such as differential input signaling (LVDS), customized input impedance and coupling type, contact Innovative sales.

Application DIO	
DIO Bits	28, arranged as 14 pairs
Signal Standards*	Single Ended: LVCMOS25 (2.5V) – **NOT 3.3V TOLERANT!** Differential pairs: LVDS25

Note: Please refer to Xilinx document DS182 “Kintex-7 FPGAs Data Sheet: DC and AC Switching Characteristics” for details on DIO signaling requirements. **Exceeding Xilinx specified absolute maximum ratings may damage the Kintex-7 FPGA and render the PEX7-COP board non-operational!**

Operating Environment Ratings

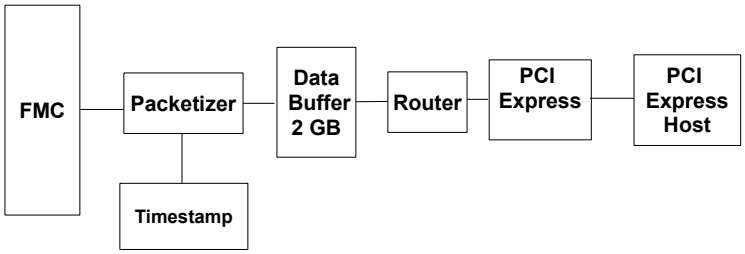
The PEX7-COP is environmentally rated L0 (office or controlled laboratory use).

PEX7-COP

Architecture and Features

The PEX7-COP architecture integrates a Xilinx Kintex-7 FPGA computing core with an FMC module on a PCI Express desktop/server three-quarter length card. Communication with the host PC is provided by a x8 Gen2 PCI Express link. The architecture tightly couples the FPGA to the FMC and enables the module to perform real-time signal processing with low latency and extremely high rates. It is well-suited for FPGA co-processing and front-end signal processing applications in wireless, RADAR and medical imaging.

Data flow between the IO and the host using a packet system



Example PEX7-COP Architecture

FMC Module

The FMC site is a VITA 57-compliant site for I/O or system expansion. The FMC module directly connects to the FPGA with 80 pairs of LVDS (160 single-ended) and 8 lanes of high speed serial. The serial lanes connect to the FPGA MGT ports.

FMC modules are integrated with the PEX7-COP by application logic in the FPGA that provides interface control and data communications. The flexible and generic nature of the FMC interface allows specialized application logic to be conveniently designed for each FMC module type.

Clocks and Triggers

Support for FMC integration with system devices includes clock and trigger sharing features so that multiple cards can perform simultaneous or coordinated sampling. Integration with a system timing card, such as Innovative X3-Timing or Atropos, allows the cards to use common sample clocks and triggers, coordinated with GPS or another system time reference.

While most Innovative FMC modules provide external clock and trigger inputs on the front panel, the PEX7-COP gives the user another option for routing the external clock, trigger and 1 PPS signals utilizing SSMC type high frequency connectors. This is useful for situations where it is desirable to keep the timing signal cabling inside the host system.

FPGA Core

The PEX7-COP family has a Kintex-7 FPGA and memory at its core for DSP and control. The Kintex-7 FPGA is capable of over 1 Tera MACs (K325 operating at 500 MHz internally) with over 1300 DSP elements in the K325 FPGA. In addition to the raw processing power, the FPGA fabric integrates logic, memory and connectivity features that make the PEX7-COP capable of performing very demanding real-time signal processing.

The FPGA has direct access to the single 2048 MB DDR3 SDRAM bank configured as 256Mb x 64. This memory allows FPGA working space for computation, required by DSP functions like FFT-s, as well as bulk data storage needed for system data buffering and algorithms like large FFT-s. A multiple-queue controller component in the FPGA implements multiple data buffers in the DRAM that is used for system data buffering and algorithm support. The DDR3 is compatible with embedded processors (uBlaze).

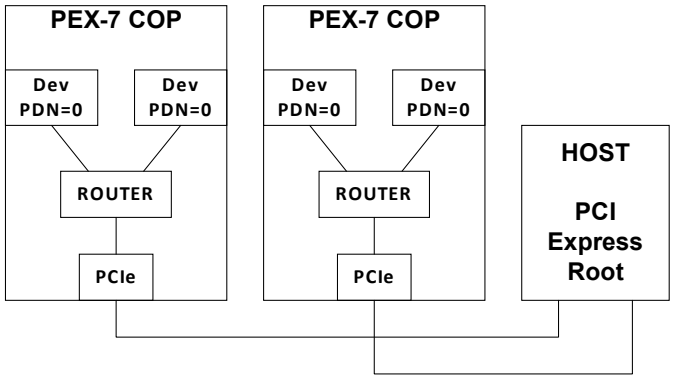
The PEX7-COP uses the Kintex-7 FPGA as a system-on-chip to integrate all the features for highest performance. As such, all I/O, memory and host interfaces connect directly to the FPGA – providing direct connection to the data and control for maximum flexibility and performance. Firmware for the FPGA completely defines the data flow, signal processing, controls and host interfaces, allowing complete customization of the functionality. Logic utilization is typically <10% of the device. Only the Clock and Trigger signals are routed outside the FPGA, using components with very low jitter and skew, to maximize analog converter performance.

Communications Interfaces

The PEX7-COP host interface features the high performance PCI Express port. This port allows the PEX7-COP to be used in many system topologies.

The PCIe port is integrated with the Velocia packet system, a powerful data network that efficiently handles data transfers between multiple, independent data sources on the PEX7-COP and the host processor. Data is packetized, using packet sizes from 32 bytes to 128KB per packet, stamped with a packet ID and destination, and then is easily routed to other devices in the system. The Velocia packet system is completely defined by the logic firmware, giving complete flexibility to create any packet routing necessary to meet system latency and transfer rate requirements.

A set of logic components for packets is provided in the FrameWork Logic including packetizer, depacketizer, router and buffer memory controls. Packetizing includes timestamping per VITA 49. Data within the packets may be any format.



Example System Topology utilizing PCIe bus

Digital I/O

The digital I/O has 28 digital lines, routed as 14 matched differential pairs, connected to the FPGA. A Samtec connector on the satellite card pins out these DIO connections. Supported I/O standards include LVCMOS25 and LVDS25.

Card Management Features

The PEX7-COP has power and health monitoring to protect the system from card failure. Independent monitoring of the FPGA die temperature can shut down the card to prevent damage from overheating. The card also has over-current protection that disconnects system power in case of failure. The FPGA also has watchdog timer functionality that may be used to recover from runaway operation.

FPGA Configuration

The modules uses a BPI FLASH memory for the Kintex-7 FPGA image. This FLASH can be programmed in-system using a software applet.

During development, the JTAG interface to the FPGA is used for development tools such as ChipScope and MATLAB. For JTAG programming either the internal USB JTAG or an external programmer such as XILINX Platform USB Cable II can be used.

Software Tools

Software development tools for the module provide comprehensive support including device drivers, data buffering, card controls, and utilities that allow developers to be productive from the start. At the most fundamental level, the software tools deliver data buffers to an application without the burden of low-level real-time control of the cards. Software classes provide C++ developers a powerful, high-level interface to the card that makes real-time, high speed data acquisition easier to integrate into applications.

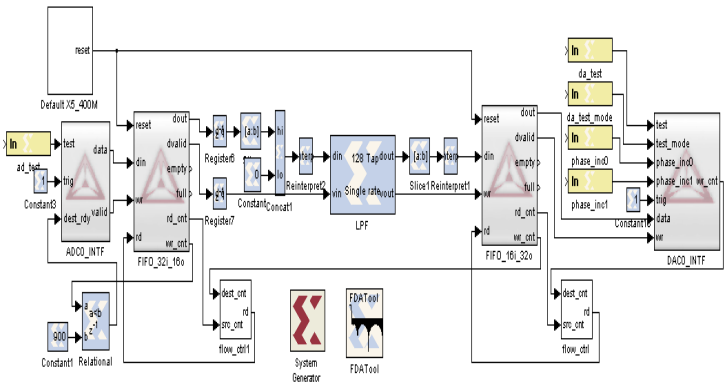
Software for data logging and analysis is provided with every module. Data can be logged to system memory at full rate or to disk drives at rates supported by the drive and controller. Triggering and sample rate controls allow use of the module's

capabilities in an application without having to write code. Innovative software applets include *Binview* which provides data viewing, analysis and import to MATLAB for large data files.

Support for the Microsoft, Embarcadero and GNU C++ toolchains is provided. Supported OSes include Windows and Linux. For more information, see the software tools User Guide and on-line help, which are available for download.

Logic Tools

High speed DSP, analysis, customized triggering and other unique features may be added by modifying the logic. The FrameWork Logic tools provide support for RTL and MATLAB developments, providing the basic hardware interfaces, data paths and controls. The standard logic provides a hardware interface layer that allows designers to concentrate on the application-specific portions of the design. A designer can build upon the Innovative components for packet handling, hardware interfaces and system functions, the Xilinx IP core library, and third party IP. RTL source for the FrameWork Logic is provided for customization. Each design is provided as a Xilinx ISE project, with a ModelSim testbench illustrating logic functionality.



Using MATLAB Simulink for Logic Design

The MATLAB Board Support Package (BSP) allows logic development using Simulink and Xilinx System Generator. These tools provide a graphical design environment that integrates the logic into MATLAB Simulink for complete hardware-in-the-loop testing and development. This is an extremely powerful design methodology, since MATLAB can be used to generate, analyze and display the internal logic signals in real-time. Once the development is complete, the logic can be embedded in the FrameWork logic using the RTL tools.

The FrameWork Logic User sales brochure and User Guide more fully detail the development tools.

IP for Kintex-7 FPGA

Innovative provides many IP cores for signal processing functions such as up/down-conversion, modulation/demodulation, OFDM receiver and transmit to name a few.

The DDC channelizers are offered in channel densities from 4 to 256. The four channel DDC offers complete flexibility and independence in the channels, while the 128 and 256 channel cores offer higher density for uniform channel width applications. The DDC cores are highly configurable and include programmable channel filters, decimation rates, tuning and gain controls. An integrated power meter allows the DDC to measure any channel power for AGC controls. Multiple cores can be used for higher channel counts.

Each IP core is provided with a MATLAB simulation model that shows bit-true, cycle-true functionality. Signal processing designers can then use this model for channel design and performance studies. Filter coefficients and other parameters from the MATLAB simulation can be directly loaded to the hardware for verification.

PEX7-COP

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