XA-TX

PCI Express XMC Module with Eight 300 MSPS DACs and Artix-7 FPGA

V0.8 3/1/17

FEATURES

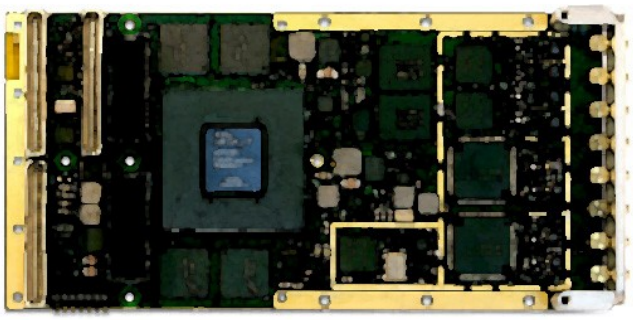
- Eight 300 MSPS, 16-bit DAC channels
- 67 dB SFDR D/As
- 1Vpp output range
- DIO on P16 (19 differential pairs)
- Xilinx Artix-7 FPGA
- DDR3 Memory
- Programmable or external sample clock
- Synchronized system sampling using common reference clock and triggers
- Framed, software or external triggering
- Log acquisition timing and events
- Power management features
- PCI Express 2.0 XMC Module (75x150 mm)
- Use in any PCI Express desktop, compact PCI/PXI, PXIe, or cabled PCI Express application

APPLICATIONS

- Wireless Transmitter
- RADAR Pulse Generation
- Arbitrary Waveform Generation

SOFTWARE

- Data Acquisition, Logging and Analysis applications provided
- Windows/Linux Drivers
- C++ Host Tools
- VHDL/MATLAB Logic Tools



The XA-TX is an XMC IO module featuring eight 16-bit, 300 MSPS DAC channels designed for high speed arbitrary waveform generation, wireless transmission, and RADAR pulse generation applications.

Flexible trigger methods include counted frames, software triggering and external triggering. The sample rate clock is either an external clock or on-board programmable PLL clock source.

Data acquisition control, signal processing, buffering, and system interface functions are implemented in a Xilinx Artix-7 FPGA device. Two 256Mx16 memories provide data buffering and FPGA computing memory.

The logic can be fully customized using VHDL and MATLAB using the FrameWork Logic toolset. The MATLAB BSP supports real-time hardware-in-the-loop development using the graphical, block diagram Simulink environment with Xilinx System Generator.

The PCI Express 2.0 interface supports continuous data rates up to 3200 MB/ s between the module and the host. A flexible data packet system implemented over the PCIe interface provides both high data rates to the host that is readily expandable for custom applications.

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This electronics assembly can be damaged by ESD. Innovative Integration recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

Product	Part Number	Description
XA-TX	80372 -<cfg> -<ruggedization>	XMC module with eight 300 MSPS DACs, Artix-7 FPGA <cfg>: 0=AC coupled, 1=DC coupled <ruggedization>: L1..L4 per Ruggedization Options table
Logic		
FrameWork Logic	55050	XA-TX FrameWork Logic board support package for RTL and MATLAB. Includes technical support for one year.
Cables		
SMA to BNC cable	67048	IO cable with SMA (male) to BNC (female), 1 meter
Options		
XMC adapters		
Data Loggers		
Embedded Computers		

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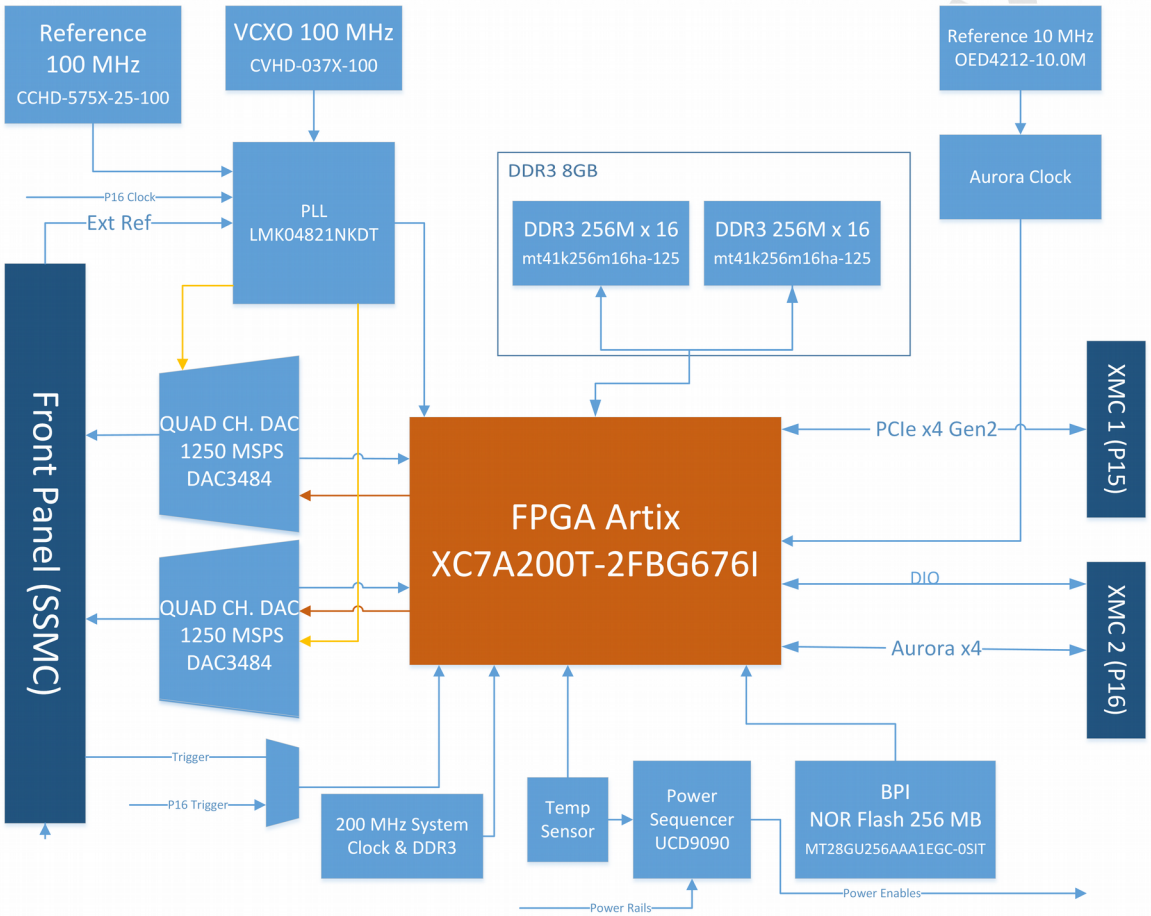
Reference
100 MHz
CCHD-575X-25-100
VCXO 100 MHz
CVHD-037X-100
Reference 10 MHz
OED4212-10.0M
Aurora Clock
P16 Clock
Ext Ref
PLL
LMK04821NKDT
DDR3 8GB
DDR3 256M x 16
mt41k256m16ha-125
DDR3 256M x 16
mt41k256m16ha-125
Front Panel (SSMC)
QUAD CH. DAC
1250 MSPS
DAC3484
QUAD CH. DAC
1250 MSPS
DAC3484
FPGA Artix
XC7A200T-2FBG676I
PCIe x4 Gen2
XMC 1 (P15)
DIO
Aurora x4
XMC 2 (P16)
Trigger
P16 Trigger
200 MHz System
Clock & DDR3
Temp
Sensor
Power
Sequencer
UCD9090
BPI
NOR Flash 256 MB
MT28GU256AAA1EGC-0SIT
Power Rails
Power Enables

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Standard Features

Analog	
Outputs	2
Output Range	+/-0.5V
Output Type	Single ended, AC or DC coupled
Output Impedance	50 ohm
DAC Device	Texas Instruments DAC3484
DAC Resolution	16-bit
DAC Sample Rate	Up to 300 MHz
Data Format	2's complement, 16-bit integer
Connector	SMA
Calibration	Factory calibrated. Gain and offset errors are digitally corrected in the FPGA. Non-volatile EEPROM coefficient memory.

FPGA	
Flip-Flops	215360
Slices	33650
Block RAM	13,140Kb Max
FPGA Device	Xilinx Artix-7 XC7A100T-2FGG676I
Configuration	SelectMAP from PCIe interface JTAG during development

Memory	
Size	2 devices @ 256Mx16 each
Type	DDR3
Uses	FPGA Buffer Memory FPGA computation memory

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Host Interface	
Type	PCI Express 2.0 eight lane
Sustained Data Rate	3200 MB/s
Protocol	Packet data
Connector	XMC P15, P16
Interface Standard	PCIe 2.0
Logic Update	In-system reconfiguration

Clocks and Triggering	
Clock Sources	PLL or External
PLL Output	44 KHz to 2000 MHz
PLL Jitter	<1 ps RMS
PLL Programming	Host programmed via PCIe
PLL Reference	Internal: 100 MHz clock External reference : J16 input
Triggering	External, software, acquire N frame
Decimation	1:1 to 1:4095 in FPGA
Channel Clocking	All channels are synchronous
Multi-card Synchronization	External triggering, clock, and PLL reference are supported.

Acquisition Monitoring	
Alerts	Trigger, Queue Overflow, Channel Over-range, Timestamp Rollover, Temperature Warning, Temperature Failure, PLL Unlocked
Alert Timestamping	TBD

P16 Digital IO	
Total Number of Bits	38
Balanced Pairs	19
Signal Standard	LVCMOS 2.5V
Drive	+/-12 mA
Connector	XMC P16

Power Management	
Temperature Monitor	May be read by the host software
Alarms	Software programmable warning and failure levels
Over-temp Monitor	Disables analog IO power supplies
Power Control	Channel enables and power up enables
Heat Sinking	Conduction cooling supported. (subset of VITA20)

Physicals	
Form Factor	Single width IEEE 1386 Mezzanine Card
Size	75 x 150 mm
Weight	TBD
Hazardous Materials	Lead-free and RoHS compliant

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ABSOLUTE MAXIMUM RATINGS Exposure to conditions exceeding these ratings may cause damage!				
Parameter	Min	Max	Units	Conditions
Supply Voltage, 3.3V to GND	0	+3.6	V	
Supply Voltage, VPWR to GND	0	14	V	
Operating Temperature	0	70	C	Non-condensing, forced air cooling required
Storage Temperature	-40	100	C	
ESD Rating	-	2k	V	Human Body Model
Vibration	-	5	g	9-200 Hz, Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04)
Shock	-	40	g peak	Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04)
RECOMMENDED OPERATING CONDITIONS				
Parameter	Min	Typ	Max	Units
Supply Voltage	3.15	+3.3	+3.45	V
Supply Voltage, Nominal 12V VPWR	11.4	12	12.6	V, unless otherwise noted specified and tested with nominal 12V VPWR
DAC Update Rate	0		300	MSPS
Operating Temperature	0		50	C

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ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at 0°C to +60°C, unless otherwise noted.

Group	Parameter	Typ	Units	Notes
Analog Outputs	Analog Output Range	+/-1000	mV	Typical, AC Coupled
		+/-1000	mV	Typical, DC Coupled
	Analog Output Bandwidth	300	MHz	DC Coupled, no sinc compensation
		300	MHz	AC Coupled, no sinc compensation
	Output Amplitude Variation	0.7	dB	0-100 MHz, DC Coupled, no sinc compensation
		0.8	dB	1-100 MHz, AC Coupled, no sinc compensation
	SFDR	67	dB	20 MHz sine output, 1.2 dBm, DC coupled
		67	dB	20 MHz sine output, 1.2 dBm, AC coupled
	SNR	TBD	dB	70.1 MHz sine output, -6 dBfs, AC coupled
	Intermodulation Distortion	72	dB	
Power	Power Consumption	12.5	A	Max
	Dissipation	22	W	Max
	Calibration Interval	TBD	year	

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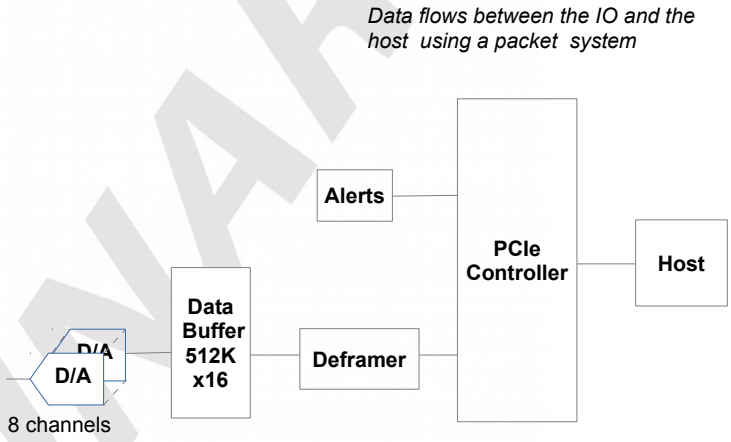
Architecture and Features

The XA-TX module has eight analog output channels of 300 MSPS, 16-bit D/A converter. The eight DAC channels have a +/-0.5V output range. Additional digital IO control bits from the FPGA are provided for application control and signaling.

Controls for triggering and clocks allow precise control over the collection of data. Trigger modes include frames of programmable size, external and software. Multiple XA-TX cards can sample simultaneously using external trigger inputs with synchronized sample clocks. The sample clock can be external or generated from the on-card PLL. The PLL can either use the on-card 100 MHz reference, or can use an external reference. When an external reference is used, the sample clock is synchronous to the reference.



XA-TX Architecture

The XA architecture has a data buffering and packet system that provides efficient and flexible data transfers to the host computer. The data buffer is a 1M sample SRAM. Data is transferred to the host using the PCIe controller interface as data packets. The packet data system controls the flow of packets to the host, or other recipient, using a credit-based system managed in cooperation with the host software. The packets may be transmitted continuously for streams of data from the DACs, or as occasional packets for status, controls and analysis results. The data buffering and flow control system delivers high throughput with low latency and complete flexibility for data types and packet sizes to match the application requirements for all types of applications.

The data acquisition process can be monitored using the XA alert mechanism. The alerts provide information on the timing of important events such as triggering, overranges and thermal overload. Packets containing data about the alert including an absolute system timestamp of the alert, and other information such as current temperature. This provides a precise overview of the card data acquisition process by recording the occurrence of these real-time events making the XA modules easier to integrate into larger systems.

Software Tools

Software for data logging and analysis are provided with every XA module. Data can be logged to system memory at full rate or to disk at rates supported by the drive and controller. Triggering, sample rate controls, and data logging features allow you to use XA modules in your application without ever writing code. Innovative software applications include *Binview* which provides data viewing, analysis and export data to MATLAB for large data files, as well as support applications for logic loading, firmware updates and system configuration.

Software development tools for the XA modules provide comprehensive support including device drivers, data buffering, card controls, and utilities that allow developers to be productive from the start. At the most fundamental level, the software tools deliver data buffers to your application without the burden of low-level real-time control of the cards. Software classes provide C++ developers a powerful, high-level interface to the card that makes real-time, high speed data acquisition easier to integrate into applications.

Support for MS Visual C++ is provided. Supported OS include Windows and Linux. For more information, the software tools and on-line help may be downloaded.

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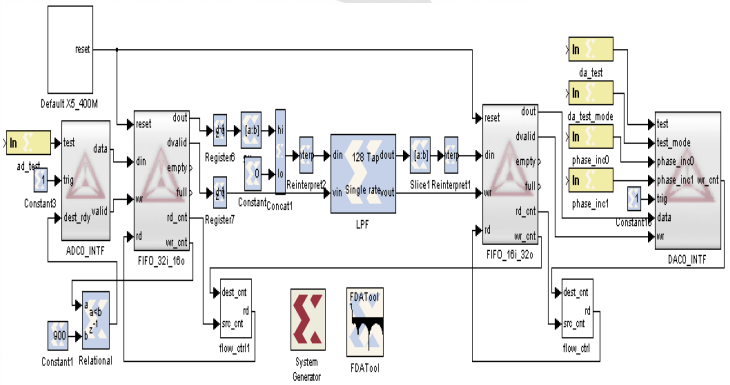
Logic Tools

High speed DSP, analysis, customized triggering and other unique features may be added to the XA modules by modifying the logic. The FrameWork Logic tools support RTL and MATLAB developments. The standard logic provides a hardware interface layer that allows designers to concentrate on the application-specific portions of the design. Designer can build upon the Innovative components for packet handling, hardware interfaces and system functions, the Xilinx IP core library, and third party IP. RTL source for the FrameWork Logic is provided for customization. Each design is provided as a Xilinx ISE project, with a ModelSim testbench illustrating logic functionality.



The MATLAB Board Support Package (BSP) supports logic development using Simulink and Xilinx System Generator. These tools provide a graphical design environment that integrates the logic into MATLAB Simulink for complete hardware-in-the-loop testing and development. The MATLAB tools are an extremely powerful design methodology that can be used to generate, analyze and display the signals in the logic real-time in the system. Once the development is complete, the logic can be embedded in the FrameWork logic using the Xilinx ISE tools.

The FrameWork Logic User sales brochure and User Guide more fully detail the development tools.

Applications Information

Maximum Data Rates

The maximum data rates supported by the module are limited by the PCI Express transfer rate when the total data rate exceeds 3200 MB/s. The PCI Express transfer rate may vary according to the host computer, operating system, and other system activity that may compete for bandwidth. The XA-TX modules supports 2400 MB/s full duplex data flow, which is within the capability of the PCIe interface.

It is important to qualify systems for performance when data rates exceeding 1500 MB/s are required.

Cables

The XA-TX module uses coaxial cable assemblies for the analog I/O. The mating cable should have an SSMC male connector and 50 ohm characteristic impedance for best signal quality.

XMC XA-TXer Cards

XMC modules can be used in standard desktop system or compact PCI/PXIe using an adapter card. The adapter cards are software transparent.

The XA modules use the auxiliary P16 connector for digital IO and additional clock inputs. A total of 8 bits of digital IO, directly connected to the application FPGA, are routed to the J16 connector as 4 balanced differential pairs supporting LVDS or lower speed single-ended LVCMOS signals. The XA modules also have a sample clock input and PLL reference input to J16. The cPCI/PXIe adapter uses these to connect to system clocks, while the PCIe desktop adapter provides SMB input connectors for system clock inputs.

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PCIe-XMC Adapter (80341) x8 PXIe to XMC Clock and trigger inputs 	**PCIe-XMC Adapter (80260)** x8 VPX to XMC Conduction cooling 	**PCIe-XMC Adapter x8 lane (80259)** x8 PCIe to XMC **x8 RIO ports supported on P16** 

Applications that need remote or portable IO can use either the eInstrument PC or eInstrument Node with XA modules.

eInstrument PC with Dual PCI Express XMC Modules (90602) Windows/Linux embedded PC 8x USB, GbE, cable PCIe, VGA High speed x8 interconnect between modules GPS disciplined, programmable sample clocks and triggers to XMCs 2000 MB/s, 4 TB datalogger 9-18V operation 	**EPC-Nano (80342)** Windows/Linux Embedded Single Board Computer Extremely small form-factor Single XMC IO Site and 1 GbE Link 8-14Vdc operation 

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