XU-TX

V 1.0 08/11/16

Innovative Integration
... real time solutions!

XMC Module with Two 6 GSPS (12 GSPS 2X) 16-bit DACs, Xilinx Ultrascale FPGA 4 GB DDR4 Memory

FEATURES

- Two 16-bit DAC channels:
  - 0.1 to 2.5GHz usable BW (standard)
  - Enhanced 2nd and 3rd Nyquist modes
  - "Frequency doubling" 2X modes
  - Single ended AC coupled outputs with programmable DC bias
  - Digital inverse sinc filter
  - 48 bit NCO
  - Fixed Latency
  - Interpolation filters: 1X(bypassed), 2X, 3X, 4X, 6X, 8X,12X,16X, and 24X
- Internal or external reference clocked
  - Internal TI LMK04821 Master Reference PLL with zero delay mode
  - Individually delay controlled reference clock to each DAC Slave PLL and FPGA
  - External Reference Input
  - Reference clock output
  - 0.054 to 6.8 GHz Slave PLL each DAC
- Advanced triggering Input
  - Registered to reference clock
- System and on-board synchronization
- Xilinx Kintex Ultrascale FPGA XCKU060
- 4GB DDR4 DRAM in 2 banks each with 64 bit interface
  - Up to 38.4GB/s total bandwidth (based on 100% data buss efficiency)

APPLICATIONS

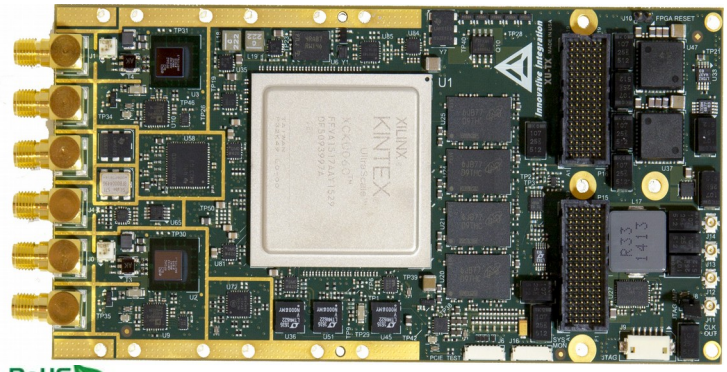
- High Speed Arbitrary Waveform Generation
- Wireless MIMO transmitter
- RADAR waveforms
- Electronic Warfare
- IP development

SOFTWARE

- MATLAB/VHDL FrameWork Logic
- Windows/Linux Drivers
- C++ Host Tools

IP Cores

- Multi-channel N-ary PSK modulator
- Chirp Generator
- AWGN Generation



RoHS 2002/95/EC Compliant

XILINX MATLAB

DESCRIPTION

The XU-TX is an XMC module with two 8 lane high speed serial links connected to the host (one on XMC connector P15, and one on P16). These links can support several protocols (up to 8 lane PCIe on P15 , Aurora, user defined, etc...). The standard XU-TX features two AC coupled single ended 16 bit DAC outputs with programmable DC bias. The Analog Devices AD9162 DAC devices employed support synchronization, interpolation, fixed latency and their unique output circuits allow improved frequency synthesis in the 2nd and 3rd Nyquist zones. This can shift the Nyquist null frequency in the output spectrum to two times the typical Nyquist null frequency.

A Xilinx Kintex Ultrascale FPGA XCKU060 with 4GB DDR4 RAM memory provides a very high performance DSP core for demanding applications such RADAR and wireless IF generation. The close integration of the analog IO, memory and host interface with the FPGA enables real-time signal processing at rates exceeding 7000 GMAC/s.

The XU XMC modules couple Innovative's powerful Velocia architecture with two high performance 8-lane PCI Express links connected to the carrier, and a new XMC carrier which connects the 8 lane XU-TX links to the 16-lane carrier PCIe link using a PCIe switch, contact the factory for availability). Alternate protocol 8-lane links to a host are also supported by the XU-TX's hardware using either P15's or P16's link to a compatible host.

The XU family can be fully customized using VHDL and MATLAB and the FrameWork Logic toolset. The MATLAB BSP supports real-time hardware-in-the-loop development using the graphical, block diagram Simulink environment with Xilinx System Generator.

IP logic cores are also available for SDR applications that provide multi-channel modulations for PSK and FSK systems. These IP cores transform the XU-TX module into versatile transmitter, ready for integration into your application.

continued on next page

XU-TX

Software tools for host development include C++ libraries and drivers for Windows and Linux. Application examples demonstrating the module features and use are provided, including streaming DAC samples from disk. The XU-TX can be used with the Andale high speed data record/playback system for arbitrary waveform generation from recorded data at sustained rates exceeding 6400 MB/s.

This electronics assembly can be damaged by ESD. Innovative Integration recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

Product	Part Number	Description
XU-TX	80335-<CFG>-<ER>	PCI Express XMC module with two channels of 6 GSPS, 16-bit DAC, 4 GB DRAM. <CFG> is configuration 0 – XCKU060-2FFVA1517E, AC-Coupled DAC <ER> corresponds to -L0, -L1, -L2, -L3 or -L4 rating from the the Ruggedization Options Table.
Logic		
XU-TX FrameWork Logic	55046	XU-TX FrameWork Logic board support package for RTL and MATLAB. Includes technical support for one year.
Cables		
SMA to BNC cable	67048	IO cable with SMA (male) to BNC (female), 1 meter
Adapters		
XMC- PCIe x8 Adapter	80259-0	PCI Express Carrier card for XMC PCI Express modules, x8 lanes
Embedded PC Host		
ePC-Duo	90602-<CFG>-<ER>	Embedded-PC XMC host with support for two XMC modules for standalone applications featuring high performance Intel i7 processor. <CFG> is configuration. <ER> corresponds to -L0, -L1, -L2, -L3 or -L4 rating from the the Ruggedization Options Table. See available options here.
ePC-Nano	80342-<CFG>-<ER>	Embedded-PC XMC host with support for singe XMC module for standalone applications featuring low-power, dual-core Intel Atom processor. <CFG> is configuration. <ER> corresponds to -L0, -L1, -L2, -L3 or -L4 rating from the the Ruggedization Options Table. See available options here.

XU-TX

Operating Environment Ratings

XU modules rated for operating environment temperature, shock and vibration are offered. The modules are qualified for wide temperature, vibration and shock to suit a variety of applications in each of the environmental ratings L0 through L4 and 100% tested for compliance. Click this link "Ruggedization Levels" to see the Ruggedization Levels available.

Minimum lot sizes and NRE charges may apply. Contact sales support for pricing and availability.

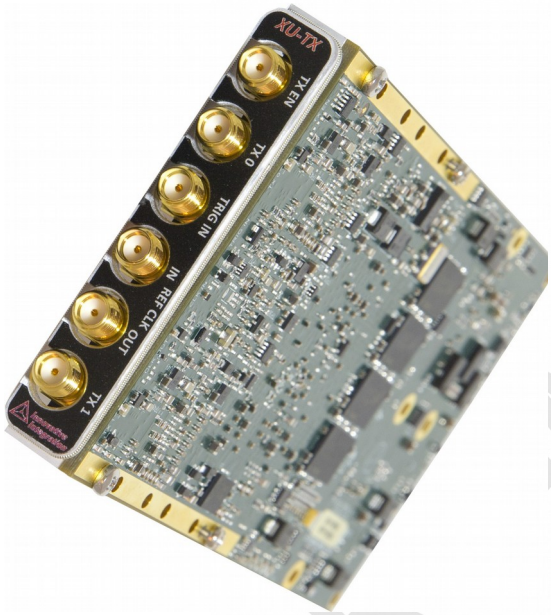


Illustration 1: XU-TX bottom, second memory bank

Illustration 2: XU-TX top, with heat spreader installed

XU-TX

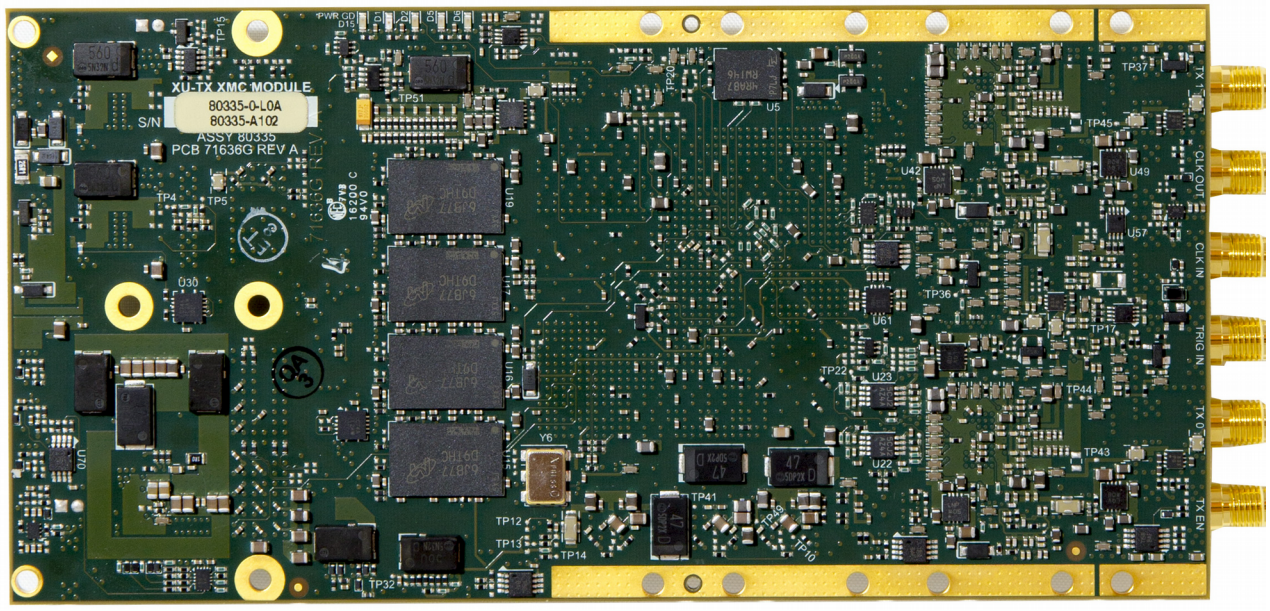
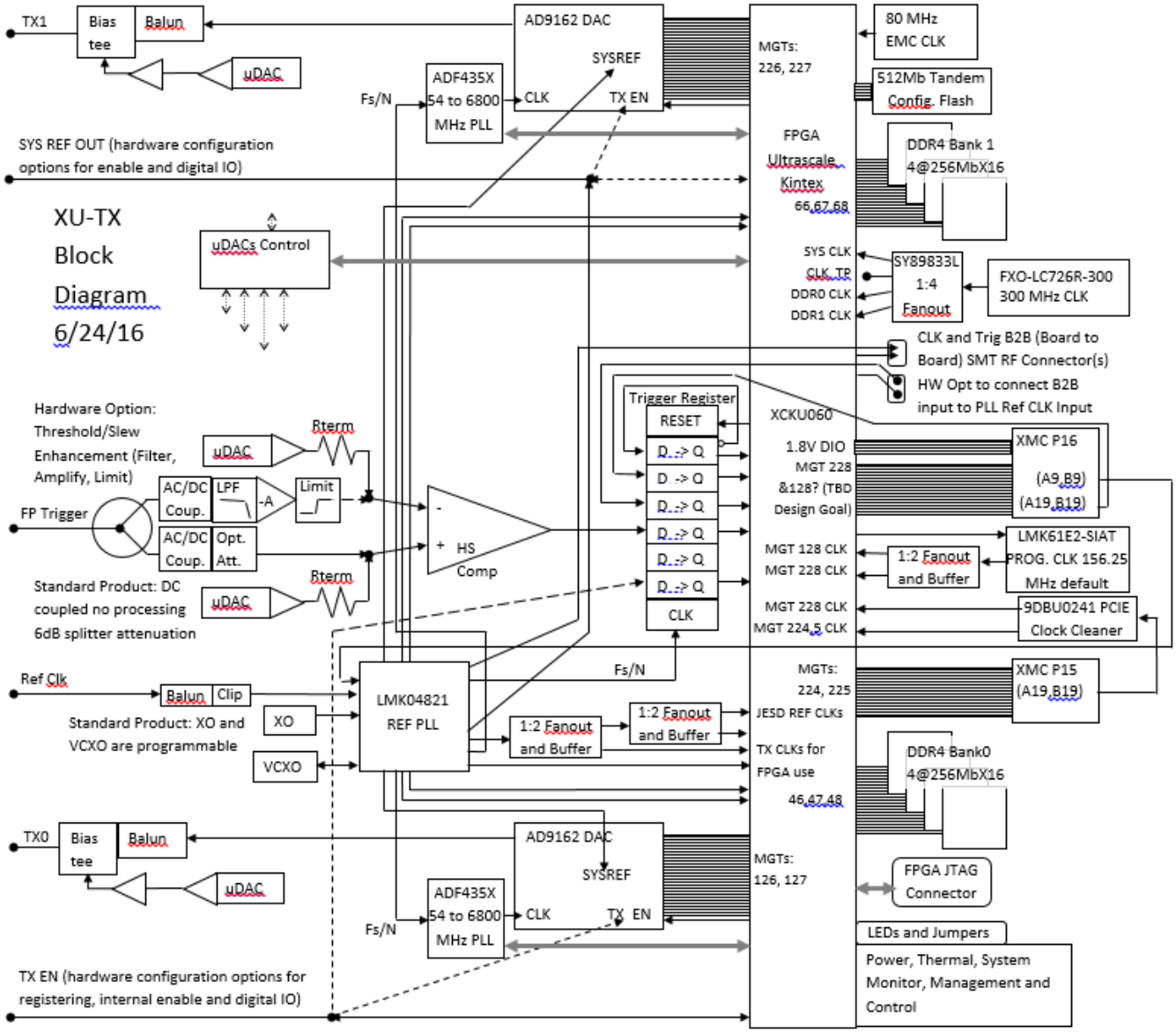


Illustration 3: XU-TX bottom

XU-TX

Functional Block Diagram



Clocking: The LMK04828 master PLL can be internally or externally referenced, provides lower speed clocks and the references for the slave microwave DAC PLLs. The LMK04828 delay control on the Slave PLLs' references can shift the delay of the slave PLLs' outputs (DAC sample clocks) locked to it, allowing delay adjustment of the DAC sample clock for synchronization. The trigger/align circuit can be used for logging a trigger signal (time stamping), and capturing the trigger input transition using a reference clock (typically sample clock divided by an integer often 8 or 16, depending on system design).

XU-TX

Standard Features

Analog	
Outputs	2
Output Range	AC: TBD > 0.6Vpp at 100 MHz DC Bias: 0 +/- 2V
Output Type	Differential
Output Impedance	50 ohm Nominal Note: The XU-TX output impedance decreases with increasing frequency due parasitic capacitance in the DAC output (a little over a pico-Farad).
DAC Device	AD9162
DAC Data Format	JESD204B
DAC IC Sample Rate	Up to 6 Gsps (up to 12 Gsps 2X DDR mode) (depending on system design)
DAC JESD 204B Rate	Up to 6 Gsps (highest speed rates are in excess of standard's maximum, but use JESD protocol) (depending on system design)
Interpolation	X1, 2, 3, 4, 6, 8, 12, 16, 24, 32 options
Modulator	Complex modulator with 48 bit dual modulus NCO
Connectors	SMA
Calibration	Factory calibrated. gain and offset errors can be digitally corrected. Non-volatile EEPROM coefficient memory.

FPGA	
Device	Xilinx Ultrascale XCKU060-2FFVA1517E
Speed Grade	-2 (commercial)
System Logic Cells	725,550
CLB Flip-Flops	663,360
CLB LUTs	331,680
Maximum Distributed RAM (Mb)	9.1
Block RAM/FIFO w/ECC (36Kb)	1,080
GTH Transceivers	32
Configuration	SelectMAP from on-board flash EEPROM - JTAG during development
Logic Utilization	TBD% FF; TBD% LUTs; TBD% BRAMs

Memories	
DRAM Size	4 GB total 8 devices @ 256Mb x16 each
DRAM Type	DDR4 DRAM
DRAM Controller	Controller for DRAM implemented in logic. Each 64 bit interface uses 2.5 FPGA I/O banks, 10@ 13 bit FPGA I/O Byte lanes (4 per bank).
Total DRAM Bandwidth	38.4GB/s maximum bandwidth (100% data buss efficiency, applications' efficiency varies)

XU-TX

Host Interface(s)	
Type	2X 8-lane high speed serial links, P15 compliant with XMC PCIe Protocol Layer Standard VITA 42.3-2006
Sustained Data Rate	System design dependent, 3.4 GBps (P15 8-lane PCIe interface with ePC-Duo) . Practical rates will be higher with goal of > 5GB/s/interface with a compatible host/connection. XU-TXs' FPGAs support optional higher speed protocols: PCIe gen2 or gen3, Aurora, user defined, etc...
Standard Protocol	8-lane PCI Express with Velocia packet system
Connectors	XMC P15, P16

Clocks and Triggering	
Clock Sources	System Reference: Ext. or Int. TCXO Master PLL: LMK0482x (used for references for slave PLLs, JESD 204B sysref, opt. trigger, etc...) Slave (DAC) PLLs 54 to 6800 MHz (depending on system design)
	External Referenc Clock Input
Jitter	Internal: TBD <350 fs rms Factory option TBD <150 fs rms (with fixed frequency VCXO)
Triggering	External, software, play N frame
Trigger	50 ohm DC coupled input, with optional programmable levels, modes
Channel Clocking	Both channels can be synchronous
Multi-card Synchronization	Within TBD (goal of <1) reference clock periods

Acquisition Monitoring	
Alerts	Trigger Start, Trigger Stop, Queue Underflow, Timestamp Rollover, Temperature Warning and Failure
Alert Timestamping	TBD: goal <= 1 reference clock periods resolution

Digital IO Connector (other interfaces have incidental and supplemental digital IO, including front and back panel clock capable digital timing IO ports)	
DIO balls, total	36
Signal Standards	FPGA 1.8V HIGH RANGE (LVCMOS18 default see Xilinx select IO user guide UG571) DIO routed as differential pairs on C# and F# except C9 and F9 which can source 1.8V up to 500mA to user circuits
Connector	P16

Temperature and Power Management	
Temperature Monitor	May be read by the host software
Alarms	Software programmable warning and failure levels
Over-temp Failure	Failure level alarm disables power
Power Control	Power good indication, and sequencing
Heat Sinking	TBD Conduction cooling (VITA20 subset) and optional fan support

Physicals	
Form Factor	Single width IEEE 1386 Mezzanine Card
Size	75 x 150 mm
Weight	TBD
Hazardous Materials	Lead-free and RoHS compliant

ABSOLUTE MAXIMUM RATINGS

Exposure to conditions exceeding these ratings may cause damage!

Parameter	Min	Max	Units	Conditions
Supply Voltage, 3.3V to GND	0	+3.6	V	4A max.
Supply Voltage, VPWR to GND	0	+14	V	8A max.
Operating Temperature	0	70	C	Non-condensing, forced air cooling required
Storage Temperature	-40	100	C	
ESD Rating	-	2k	V	Human Body Model (handled by edges, internal circuit nodes may be more sensitive)
Vibration	-	5	g	9-200 Hz, Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04)
Shock	-	40	g peak	Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04)
RECOMMENDED OPERATING CONDITIONS				
Parameter	Min	Typ	Max	Units, Conditions
Supply Voltage, 3.3V to GND	3.15	3.3	3.45	V
Supply Voltage, Nominal 12V VPWR	11.4	12	12.6	V, unless otherwise noted specified and tested with nominal 12V VPWR
Supply Voltage, VPWR Range	+7.5*	+14	V	V, 8A max. *Rev.A, Rev B goal +4.25 V Min
Operating Temperature	0		50	C
Forced Air Cooling	TBD			Approximate 200 LFM
Specification and Test clock frequencies	TBD (5?)			GHz

Note: XU-TX specifications and test is based on industry standard and critical component vendor test methods, which allows trace-ability to the components' test and supported operation, easier product comparisons, etc... Operation or test other ways; increasing FFT points, different sample rates and input frequencies, etc... may void the applicability of this specification... and/or require an application specific system design, consult the factory for specific needs,.

Raw Performance Typical Plots TBD

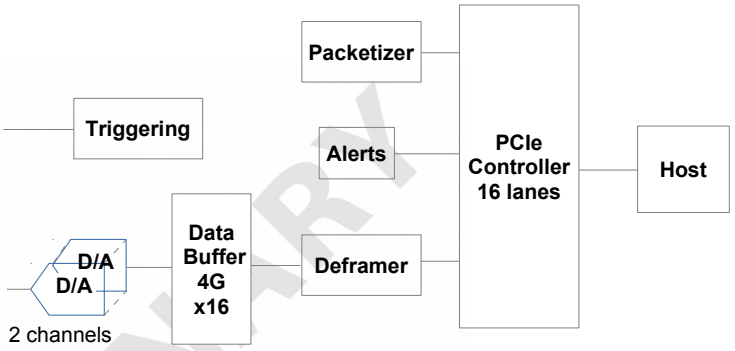
Single Tone	Other Single Tone
Noise floor, AC Coupled	Dual Tones
AC Coupled SNR vs Output Frequency	AC Coupled SFDR vs Output Frequency

XU-TX

Architecture and Features

The XU-TX module architecture integrates analog IO with an FPGA computing core, memories and two XMC VITA 42.3-2006 PCI Express protocol compliant 8-lane host interfaces. This architecture tightly couples the FPGA to the analog and enables the module to perform real-time signal processing with low latency and extremely high rates. The XU-TX is ideal as a front-end for demanding applications for complex signal generation used in wireless transmitters, RADAR, and electronic warfare applications.

Data flows between the IO and the host using a packet system



XU Architecture

Analog IO

The analog front end of the XU-TX module has two DAC outputs, which can be simultaneously updated (default) and synchronized to 4 DAC clock periods (preliminary, design goal to reduce). The DAC devices employ unique output circuits which allow improved frequency synthesis in the 2nd and 3rd Nyquist zones. This can shift the Nyquist null frequency in the output spectrum to two times the typical Nyquist null frequency.

The DAC features programmable interpolation, filtering and mixing to support frequency digital upconversion (DUC) of the baseband waveform. The DUC features take lower speed baseband signals and upconvert them to high speed IF, significantly unburdening the FPGA processing for many communications and RADAR signal applications. The DAC has a complex modulator with a 48 bit dual modulus NCO.

The DUC features are controlled through the FPGA and may be completely bypassed to use the DAC in simple mode.

Or the DAC NCO can be configured to generate a sinusoidal signal on the DAC output without using memory or streamed data.

The DAC channels operate synchronously for simultaneous DAC updates using the PLL which can be referenced to external timing input(s). Trigger modes include frames of programmable size, external and software. Multiple cards can play simultaneously by using external trigger inputs and clock. The trigger component in the logic can be customized to accommodate a variety of triggering requirements.

Understanding the advanced DAC Features and Modes…

The XU-TX DACs have advanced modes of operation which make them much more flexible but therefore harder to specify. Below is a conversation focusing on the DACs used in the XU-TX...

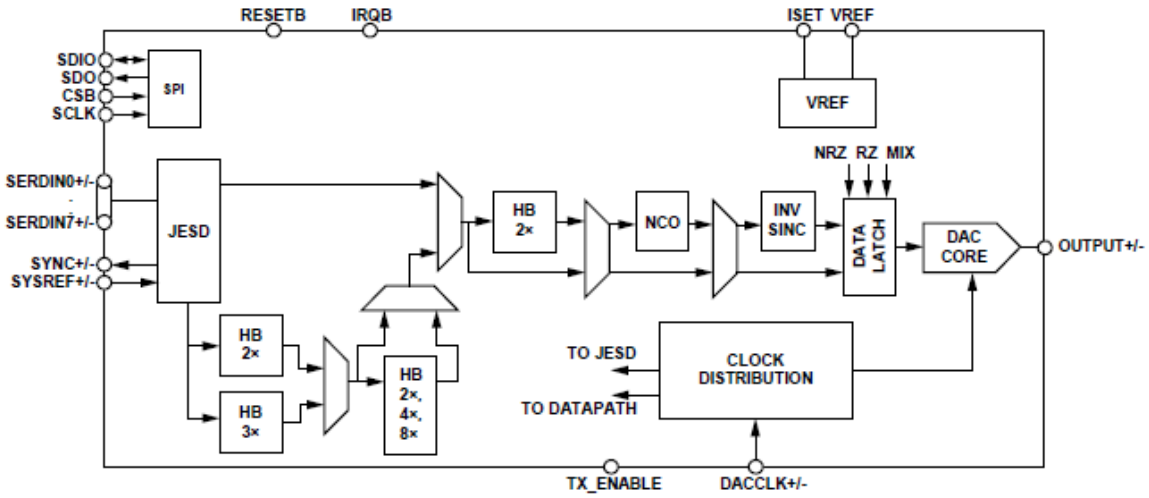
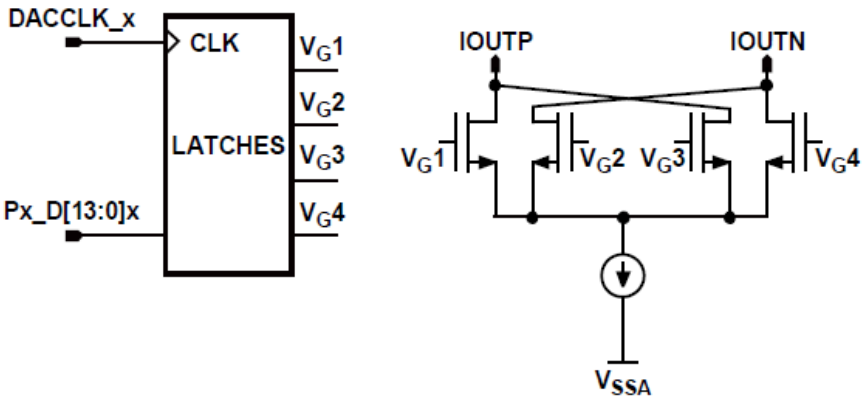


Figure 1.

Much of the XU-TX DACs' samples' digital pre-processing is well understood and common in modern DACs, but is made more powerful as it is combined with some hardware enhancements...

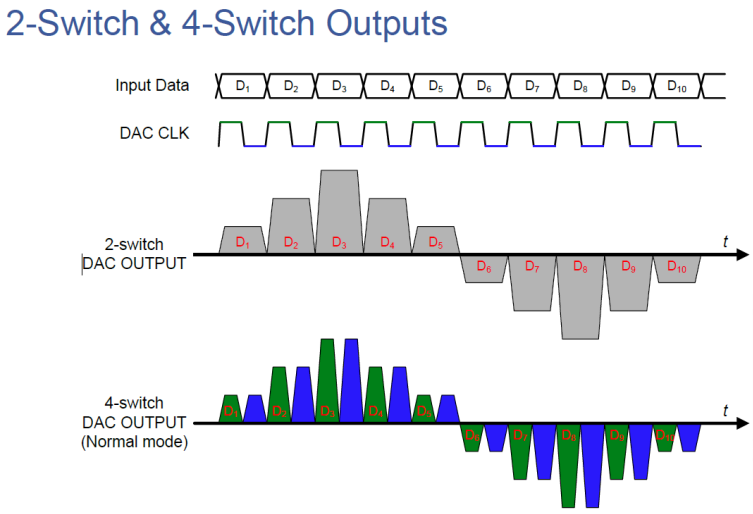
An enhancement to the DAC output which allows reduced code dependent distortion is the quad switch output architecture....



In the older two switch approach, if the DAC output current element did not change state for a given sample the switch FETs (Field Effect Transistors) would not switch. When these FETs switch there is an unavoidable "glitch" in the DAC output, and so one might think not switching is good, except that the switching glitch is then output code dependent which results in code dependent distortion. With the quad switch architecture there can be a two switch glitch every update even if the code for this current source element does not change, and the "glitch" is not code dependent, improving distortion. However having this 2 switch glitch every update does create a significant clock spur at twice the DAC clock rate in the output spectrum.

The AD9162 uses the quad switch output and can sample on the rising and falling edge of the clock effectively doubling the input clock,

locking at the output with and without the doubled sample clock....



When used with 2X interpolation this can effectively double the, for example, 6 Gsps sample update rate from the FPGA to generate a 12 Gsps 2X interpolated DAC output.

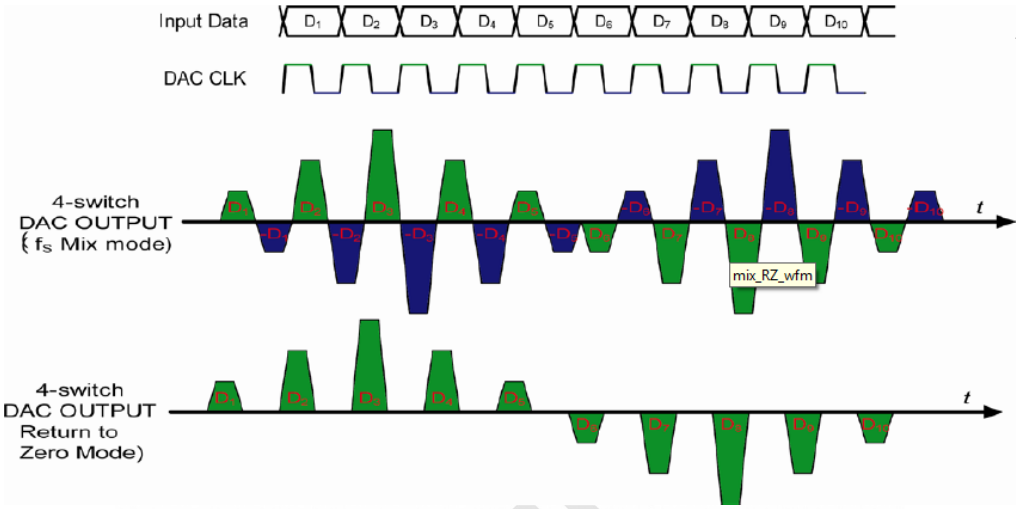
The DAC also has a “shuffle mode”, while the details of this are still proprietary, “shuffle” implies the redundant DAC output current source elements, and perhaps references, are “shuffled” so any error (time or amplitude) associated with a given element or level is not repeated in a pattern, which would show up as frequency spur in the output. “Shuffling” does not reduce real harmonics due to simple non-linearity and is typically beneficial in higher frequency applications where the timing errors and high frequency parasitic effects cause mismatchs, which tend to dominate SFDR (Spurious Free Dynamic Range). Shuffling works best with some back off from DAC full scale operation as closer to full scale there is a higher utilization of, and less alternate combinations of, output resources available to shuffle for a given output code/level. Shuffling generally “spreads” spurs out in the frequency domain with a random selection algorithm keeping them from being periodic in time and therefore keeping them from contributing higher level spur(s) in the frequency domain. So shuffling will typically incur a 1 to 3 dB noise floor penalty depending on power of the spurs being spread which is redistributed as “noise”.

XU-TX

DAC output modes comparison

The DAC block diagram shows the controls for three modes labeled “NRZ”, “RZ” and “MIX” which are supported by the DAC output.

Two enhanced output modes are “RZ” (Return to Zero also called pulsed) and “MIX” modes...



In the frequency domain the traditional “NRZ” (Ts = Ton) mode can be generalized for the “RZ” (0 < Ton ≤ Ts) mode Fourier transform (based on “Advanced Data Converters” by Gabrele Manganaro)...

$$\mathbf{iout}(f) = \mathbf{Iout}(f)\left[\sum_{n=-\infty}^{+\infty} \partial(f - n \cdot fs)\right]\frac{Ton}{Ts}e^{-j\pi Ton}sinc(fTon)$$

for the Ton = 0.5Ts case supported by the XU-TX’s DAC we can see 2Ton =Ts = 1/(fs) or Ton = 1/(2fs), given...

sinc(πfTon) = sin(πfTon) / (πfTon) = sin[πf/(2fs)] / [πf/(2fs)]

The Nyquist nul is shifted to 2fs for Ton = 0.5Ts as compared to fs for the traditional DAC Ton =Ts case.

And the low frequency amplitude of the output (were sinc(πfTon) ≅ 1 for both cases) is scaled by the duty cycle D = Ton/Ts = 0.5

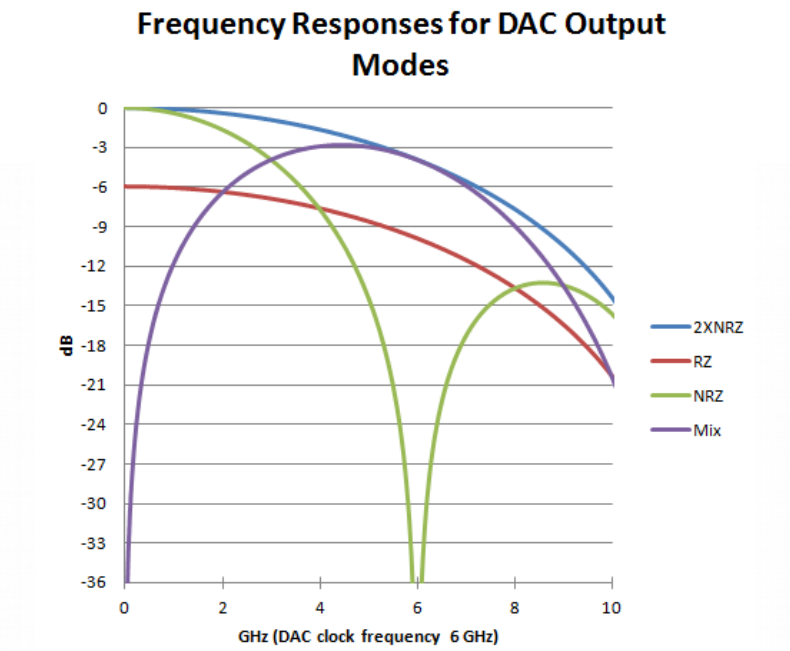
In the frequency domain using the “RZ” D=1/2 mode result as a basis the “mixed” mode Fourier transform (based on “Advanced Data Converters” by Gabrele Manganaro)....

$$\mathbf{iout}(f) = 2\mathbf{Iout}(f)\left[\sum_{n=-\infty}^{+\infty} \partial(f - n \cdot fs)\right]\frac{1}{2}e^{-j\pi f/(2fs)}sinc\left(\frac{f}{2fs}\right)e^{-j\frac{\pi}{2}(1+\frac{f}{fs})}\cos\left[\frac{\pi}{2}\left(1+\left(\frac{f}{fs}\right)\right)\right]$$

The “RZ” mode “Sinc distortion” is multiplied by a shape function, the result of which has increasing power into the second Nyquist band which can, for example, provide some cable equalization if used in some of the higher frequency XU-TX output circuit options.

Plotting the supported modes.(Note this is unfiltered, ideal, digital, does not include the DAC output and circuit effects)...

Ideal Digital



"NRZ" (Non-Return to Zero) is the traditional DAC mode... The output will have a traditional Sinc frequency response, which can be digitally flattened up to about 40% of the sampling rate with an inverse sync filter built into the DAC (typically 3.8 dB loss and +/-0.05 dB flatness in the digital signal, as we will see later, BW and flatness are effected by the circuitry on and connected too the DAC outputs)...

"2XNRZ" is the 2X "DDR" clocked 2X interpolated output which doubles the Nyquist nul frequency of the "NRZ" traditional DAC mode.

The XU-TX DAC also supports **"RZ" (Return to Zero)** mode with a duty cycle of ½ (the output is pulsed "on" for Ton which is ½ of each Ts sampling period). This "RZ" (Return to Zero) mode has trade offs (approximately -6dB (½ amplitude) compared to "2XNRZ" mode) but is generally accepted as an analog performance enhancement to the traditional DAC "NRZ" when operating at higher frequencies.

As the DAC clock frequency increases the DAC output settling time takes a larger percentage of the sample period, and this settling can be non-linear or asymmetrical adding impairments which depend on the specific output code transition. Also parasitic elements, delays and "strays" have a larger impact on circuit operation and balance making the output transitions less ideal at higher frequencies. This introduces non-linear inter-code interference in a NRZ DAC mode. However in a RZ DAC mode all transitions are from and to "zero" and have little or no memory of the prior output code which reduces non-linear inter-code interference and the associated output distortion.

"Mix" mode has a different frequency shaping function and can be thought of as "chopping" (modulating) the DAC output at the DAC sample rate shifting the output power to near the sample rate.

Comments on jitter effects on output modes

Mostly theory taken from "Radio Frequency Digital to Analog Converter" Susan Luschas pHD Thesis Massachusetts Institute of Technology 2003

One of the main SNR (Signal to Noise Ratio) limits of microwave DACs is the DAC clock jitter limit. Traditional "NRZ" mode is typically

best at lower frequency (1st Nyquist zone). “RZ” mode has performance benefits at higher frequency. Mixed mode is likely a compromise between the above.

Intuitively a traditional “NRZ” DAC’s current sources can have 0, 1 or 2 code transitions associated with a sample code, and different numbers of different value current source elements can change with each transition (depending if the sample code is different, and different by a lot or a little, from the code before or after) which with a jittered transition adds uncertainty with each transition degrading the possible SNR, the aggregate uncertainty increases with the amount and rate of output change (and therefore frequency and sampling rate of the output). Another way to think of the sampling rate effect is as the sample period shrinks and transitions become more frequent, the random jitter variation in the clock seen on each transition is seen in the output in a larger number of transitions...

In a traditional “NRZ” DAC / typical system, jitter is not typically a limiting SNR factor with low output frequencies (fout <<fs) where change per. sample is relatively small. As the output frequency increases the achievable SNR for a fixed amount of jitter decreases with fout.

If the sampling frequency is increased proportionally with the output frequency, the achievable SNR for a fixed amount of jitter still decreases with the square root of fout. So the SNR jitter limit will still get worse if the sampling rate is increased with the output frequency (same number of samples for a given output waveform, and same amount of jitter).

However a RZ DAC mode is always going to have the same number of transitions (except perhaps arguably transitions at zero output, where the transition effects will be small regardless (from zero to zero)) and the transitions will be the same amplitude for a given code (two each; one from and one to zero).

So while worse at lower output frequencies, the RZ mode jitter limited SNR is relatively independent of the changes between output codes, and therefore the change rate and therefore frequency of the output waveform. RZ mode is also relatively independent of the number of DAC bits.

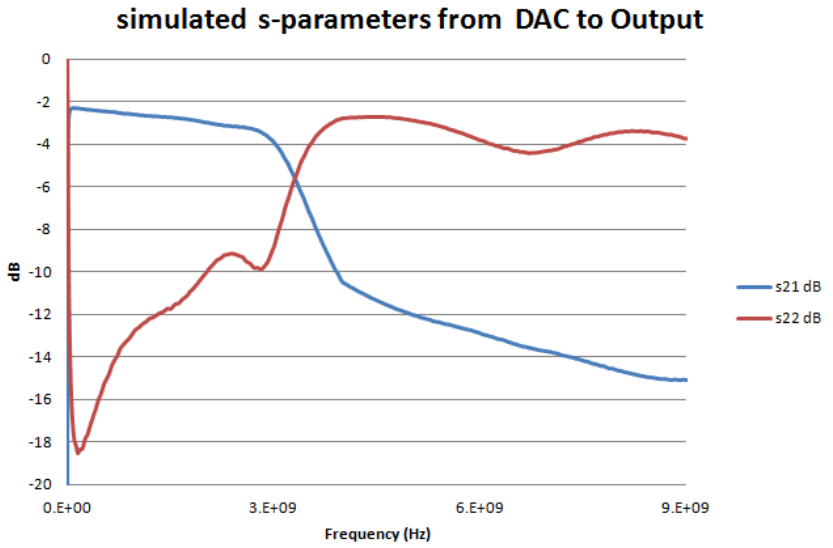
Below the Nyquist sampling rate the NRZ mode will typically be better for Jitter limited SNR. Near Nyquist sampling the NRZ jitter SNR limit is still expected to be 3 dB higher than RZ mode. So RZ mode may make sense for higher frequency uses with, for example, relatively arbitrary waveforms, and where other SNR factors, or system metrics (such as non-linear code interference distortion SFDR concerns) dominate the jitter limited SNR.

The author could not find a definitive result for mixed mode and can see how a mixed mode device could be designed as a combination of RZ node devices or a modulated NRZ mode, so suspects the Mixed mode with frequency doubling to fall between the two, perhaps closer to RZ mode. As while it is not zero rate at transitions between values, it is closer to zero value RZ than NRZ mode.

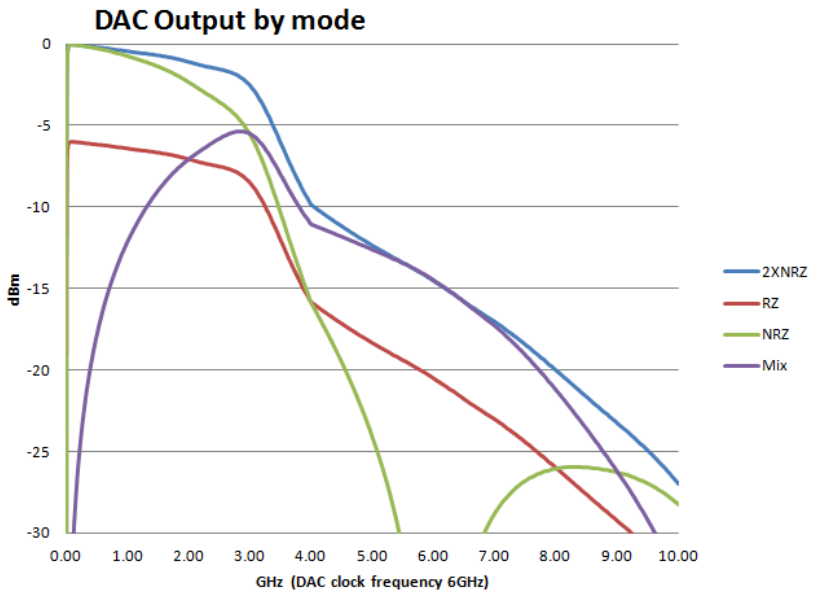
DAC to Output “front end” circuit frequency response

From the DAC the output “front end” circuit on the XU-TX converts the DAC output currrent to a single ended Voltage output with a transformer... The standard XU-TX product’s simulated response (includes the analog components in the DAC)...

The DAC return loss degrades with increasing frequency due the parasitic capacitance in the DAC output, (a little over a pF which effectively shorts the DAC complementary outputs together with increasing output frequency). Also while all XU-TX products are AC coupled, a low frequency bias DAC on the XU-TX can used with a bias tee to provide a DC levels on the outputs.



Putting the above analog and digital frequency responses together with conservative output level we get the standard product's simulated supported frequency spectrum for the different DAC modes for a sinusoidal signal... For the standard XU-TX...



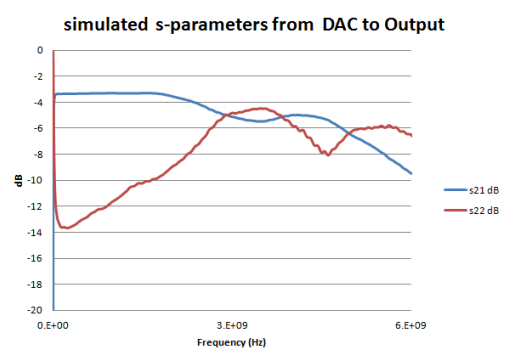
Note: digital signal pre-processing can be employed; inverse sinc filtering built into the DAC, as an example, could be used to flatten the NRZ mode spectrum to the S21 curve up to 0.4 fdac or for the 2XNRZ mode up to 0.8 fdac with added insertion loss of about 3.8dB, etc...

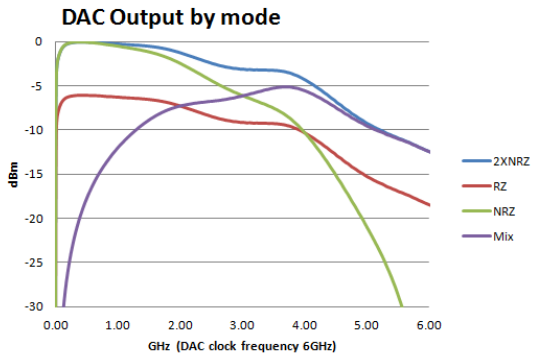
Higher frequency output future options (contact factory)...

As seen above the standard option is usable to 3 GHz. Two other non-standard transformers were allowed for to take advantage of the higher frequency capability of the DAC used. Though it is noted that the return loss of the DAC and therefore the XU-TX output degrades due the parasitic capacitance in the DAC output at higher frequencies...

Mid frequency future analog bandwidth option

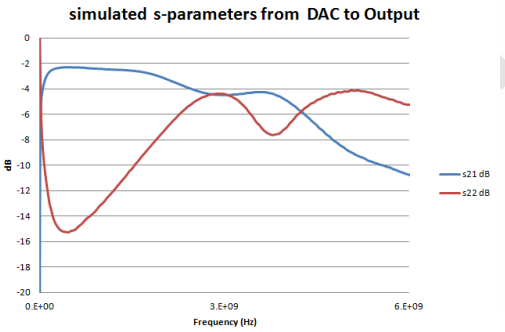
Analog frequency response and supported frequency spectrum for the different DAC modes for a sinusoidal signal...

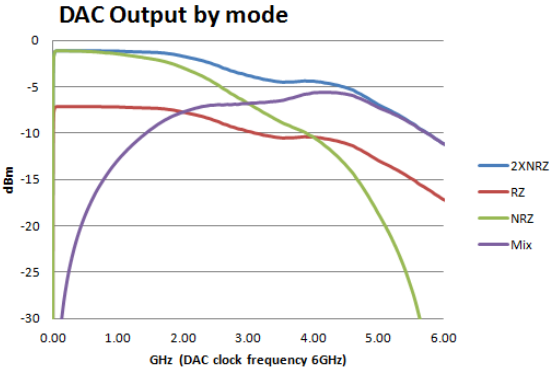




High frequency future analog bandwidth option

Analog frequency response and supported frequency spectrum for the different DAC modes for a sinusoidal signal...





Analog bandwidth options notes:

The standard product's transformer performs well from 10 MHz to 2.25 GHz (note other circuit components roll the XU-TX frequency response off below 100 MHz). Above 2.5 GHz phase imbalance may impact distortion performance.

The mid-frequency future option frequency response extends down to low frequencies but the amplitude and phase imbalance will result in increased distortion levels at lower frequencies. The transformer is specified from 650MHz to 4 GHz and the "sweet spot" is from 1 GHz to 3.5 GHz.

The high-frequency future option, while the widest BW, is expected to have slightly worse distortions, noise and signal level compared to the lower frequency options in their respective target bands.

FPGA Core

The XU Module family has a Xilinx Ultrascale FPGA and memory at its core for DSP and control. An XCVU065T or XCVU095 FPGA are available. The Xilinx Ultrascale FPGA is capable of 8180 GMACs (XCVU065T operating at 800 MHz internally), about 200x faster than traditional DSPs. In addition to the raw processing power, the FPGA fabric integrates logic, memory and connectivity features that make the FPGA capable of applying this processing power to virtually any algorithm and sustaining performance in real-time. The FPGA has direct access to the DDR4 DRAM. These memories are used as FPGA working space for computation, required by DSP functions like FFTs, and bulk data storage needed for waveform calculations. A multiple-queue controller component in the FPGA implements multiple data buffers in the DRAM that is used for system data buffering and algorithm support.

The XU module family uses the Xilinx Ultrascale FPGA as a system-on-chip to integrate all the features for highest performance. As such, all IO, memory and host interfaces connect directly to the FPGA – providing direct connection to the data and control for maximum flexibility and performance. Firmware for the FPGA completely defines the data flow, signal processing, controls and host interfaces, allowing complete customization of the XU module functionality.

System and use case factors which may impact maximum sample stream rates....

The DACs sample streams' TB ("total bandwidth") is...

TBdac = (number of DACs) (bits/sample) (sample rate)

TBdacMax = (2) (16 bits/sample) (6 Gsps) = 192 Gbps

Notes:

Possible coding is not included in TBdac as for the current purposes it is transparent to the user (added and removed by the JESD204B interfaces).

DAC JT (junction temperature) of 105 degrees Celsius is assumed, the DACs can be slightly overclocked with lower JT

DDR4 memory bandwidth

The XU-TX has high speed DDR4 memory available for the user. Two of the more common use cases are....

Streaming samples from the DDR4 to the DACs with one memory access per. sample (on each of the two memory interfaces). For example if we write the waveforms sample data into the DDR4 memories (once prior to streaming) and then stream reading the samples from the DDR4 to the DACs during streaming)

Using the memory to process samples for each DAC with two memory accesses per. sample (for example a FIFO which writes and reads one sample value to/from the DDR4 for each DAC sample (the actual high efficiency implementation would typically be bursts of writes and reads as this is more optimum for the memory system's bandwidth)).

The DDR4s are in two 64 pin banks with each bit having a maximum transfer rate of 2.4 Gbps per. bit (2.4 gigabits per. second maximum as XU-TX uses a speed grade 2 FPGA).

DDR4 memories are never 100% efficient, actual efficiency depends on a number of system factors, and is therefore application / system design dependent. In this discussion an efficiency of 91% will be used, to reflect a relatively simple ideal streaming system.

TBddr = (number of interfaces) (pins/interface) (maximum bit rate/pin) (efficency) / (memory accesses per. bit)

For one memory access

TBddrMax = (2) (64 bits) (2.4 Gbps) (91%) / (1) = 279.552 Gbps > 192 Gbps = TBdacMax

So full rate DAC streaming is possible.

For two memory accesses

TBddrMax = (2) (64 bits) (2.4 Gbps) (91%) / (2) = 139.776 Gbps < 192 Gbps = TBdacMax

So full rate DAC streaming is not possible, streaming is limited to approximately 4.368 Gsps with two DACs operating, and the maximum sampling rate can decrease with lower efficiency memory usage.

It may be possible to stream up to the maximum 6Gsps rate from memory to one DAC using both memory interfaces for one DAC with two memory accesses per. sample in some system designs.

XMC connector and carrier bandwidth

Another possible use case is streaming from the XMC interface. Half the XMC interface lies on the carrier which the XU-TX plugs into through the XMC connectors. The XMC link performance depends on the intgeraction of the XU-TX, the carrier and link between them (the most bandwidth restrictive part of which is typically the XMC connectors). An XMC carrier available at the time of writing, likely to be used with the XU-TX indicates 3.4 GBps (27.2 Gbps) sustained PCIe over XMC BW (ePC-Duo).

At the time of writing overclock the XU-TX PCIe is expected to exceed the standard speed and PCIe "generation" of the connectors used, but has not been tested and depends on system design). Also a future XU-TX option is to use XMC 2.0 connectors. XMC connectors are built to Vita 42, and XMC 2.0 connectors are built to VITA 61. While printed circuit board compatible (following is a comparison table from ANSI/VITA 61.0-2011 (R2014)). ….

Table 5-1: PCIe to VITA Connector Comparison

	PCIe		
	Gen1[3]	Gen2[3]	Gen3[3]
VITA 42 (3.125 Gbaud[1])	2.5Gbaud	5Gbaud	8Gbaud
VITA 61 (7.5 Gbaud[2])	2.5Gbaud	5Gbaud	8Gbaud

[1] Application Note: SamArray® YFT/YFS Final Inch™ Designs in RapidIO Short Run(Mezzanine) Applications, XMC Connector, 10mm Stack Height
[2] Presentation: VITA 61 XMC 2.0 Update, Mezalok Stacking Connector, March 9, 2011, Tyco Electronics
[3] VITA 68.0, VPX Compliance Channel, Revision 0.27, 01 September 2011, Table 4.1-1

Current carriers should be able to support streaming to both DACs from the XMC interface at up to 0.85 Gsps and future carriers should support 2X this or 1.7 Gsps.

It may be possible to stream 1.7 Gsps now, to one DAC using the full PCIe over XMC BW for one DAC in some system designs.

Note: the possible system limits in the data stream system use cases described above have less of an output BW impact with the innovative DAC used on the XU-TX, as these do not impact the frequency response from the DAC to output (s21) and the reduced DAC output frequency spectrum response can be, for example, doubled as compared to a traditional DAC by using a DDR 2X clock with 2X interpolation doubling the effective output bandwidth as compared to a traditional DAC without these enhancements.

Additional passive board to board, "break-out" or other extending interfaces' bandwidth

Some system designs may use additional interfaces in series, such as XMC to PCIe adapters or extenders without reconditioning the signals. Naively modeling board to board connectors the signal pin contact is typically inductive and the pads to mount the pin contacts on both boards are typically capacitive... so naively a board to board connection can be seen as a "PI" low pass filter section. Likewise transmission lines between the interfaces typically have increasing attenuation as a function of frequency (effectively low pass filters) and connecting these in series will typically reduce the link's end to end bandwidth (and may add undesired resonances to the frequency response). XU-TX was designed to minimize these effects, as practical, but the XU-TX is one of three or more interacting boards in such a composite link, and there will likely be some reduction in bandwidth (and possibly increase in jitter and lane skew) the system designer should allow for. A common rule of thumb is the composite link should have a simple gradual monotonic roll-off with frequency, and less than seven deciBels of loss from end to end at the fundamental frequency (the link lane's raw bit rate divided by two), but this also depends on the host transceiver's capability.

PCI Express Host Interface

The XU architecture supports a 8-lane PCI Express link from the host, which can be sourced from a 8-lane PCI Express link on the host using the Velocia packet system. The Velocia packet system is an application interface layer on top of the fundamental PCI Express interface that provides an efficient and flexible host interface supporting high data rates with minimal host support. Using the Velocia packet system, data is transferred to the host as variable sized packets using the PCIe controller interface. The packet data system controls the flow of packets to the host, or other recipient, using a credit system managed in cooperation with the host software. The packets may be transmitted continuously for streams of data to the DACs, or as occasional packets for status, controls and analysis results. For all types of applications, the data buffering and flow control system delivers high throughput with low latency and complete flexibility for data types and packet sizes to match the application requirements. Firmware components for assembling and dissembling packets are provided in the FrameWork Logic that allow applications to rapidly integrate data streams and controls into the packet system with minimum effort.

The XMC PCI Express protocol interfaces are implemented in the Xilinx Ultrascale FPGA using a link with 8 GTH lanes each. The XU-TX FPGA supports PCIe gen 3, and the PHY supports future projected gen 4 rates, so rates will typically be limited by the XMC host / connection. Since PCI Express is not a shared bus but rather a point-to-point channel, system architectures can achieve high sustained data rates between devices – resulting in higher system-level performance and lower overall cost.

Private Data Links

The XU module family can support private data links on the P15 or P16 connector (assuming a host interface on the other connector) that can be used for system integration. The XMC P15 and P16 connectors each have 8 lane links connected to FPGA GTH transceivers. The GTH lanes can be used to provide low-latency, high rate data to the system in addition to the PCI Express interface. Maximum data rates, with deterministic performance can be implemented in performance-driven systems using little or no protocol. For more complex systems, protocols such as Aurora can be used.

Module Management

The data acquisition process can be monitored using the XU alert mechanism. The alerts provide information on the timing of important events such as triggering, over-ranges and thermal overload. Packets containing data about the alert including an absolute system timestamp of the alert, and other information such as current temperature. This provides a precise overview of the card data acquisition process by recording the occurrence of these real-time events making the XU cards

easier to integrate into larger systems.

FPGA Configuration

The XU modules have configuration FLASH that can hold multiple FPGA application images. In addition to the application image(s), a "golden" image is kept in FLASH for disaster recovery. The FLASH can be reprogrammed in-system using a software applet for field upgrades.

During development, the JTAG interface to the FPGA is used for development tools such as ChipScope and MATLAB. The FPGA JTAG connector is compatible with Xilinx cables such as Platform USB Cable.

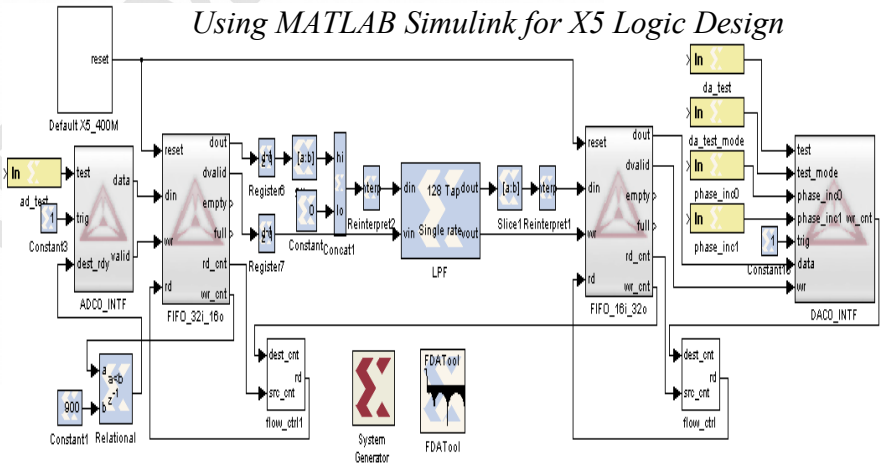
Software Tools

Software development tools for the XU modules provide comprehensive support including device drivers, data buffering, card controls, and utilities that allow developers to be productive from the start. At the most fundamental level, the software tools deliver data buffers to your application without the burden of low-level real-time control of the cards. Software classes provide C++ developers a powerful, high-level interface to the card that makes real-time, high speed data acquisition easier to integrate into applications.

Example software for data playback and and card control are provided with every XU module. Data can be played back from system memory at full rate or from disk drives at rates supported by the drive and controller. Triggering and sample rate controls allow you to use the XU performance in your applications without ever writing code. Innovative software applets include *Binview* which provides data viewing, analysis and import to MATLAB for large data files.

Support for MS Visual C++ and QtCreator are provided. Supported OS include Windows and Linux. For more information, the software tools User Guide and on-line help may be downloaded.

Logic Tools



High speed DSP, analysis, customized triggering and other unique features may be added to the XU modules by modifying the logic. The FrameWork Logic tools provide support for RTL and MATLAB developments. The standard logic provides a hardware interface layer that allows designers to concentrate on the application-specific portions of the design. Designer can build upon the Innovative components for packet handling, hardware interfaces and system functions, the Xilinx IP core library, and third party IP. RTL source for the FrameWork Logic is provided for customization. Each design is provided as a Xilinx ISE project, with a ModelSim testbench illustrating logic functionality.

The MATLAB Board Support Package (BSP) allows logic development using Simulink and Xilinx System Generator. These tools provide a graphical design environment that integrates the logic into MATLAB Simulink for complete hardware-in-the-loop testing and development. This is an extremely power design methodology, since MATLAB can be used to generate, analyze and display the signals in the logic real-time in the system. Once the development is complete, the logic can be embedded in the FrameWork logic using the RTL tools. The FrameWork Logic User sales brochure and User Guide more fully detail the development tools.

XU-TX

Application Information

Cables

The XU-TX module uses coaxial cable assemblies for the analog IO. The mating cable should have a male connector and 50 ohm characteristic impedance.

XMC Adapter Cards

XMC modules can be used in standard desktop system or compact PCI/PXI using a XMC adapter card. An auxiliary power connector to the PCI Express adapters provides additional power capability for XMC modules when the slot is unable to provide sufficient power. The adapter cards allow the XMC modules to be used in any PCIe or PCI system.

The XU-TX XMC modules couple Innovative's powerful Velocia architecture with two high performance 8-lane PCI Express links connected to the carrier, and a new XMC carrier which connects the 8 lane XU-TX links to the 16-lane carrier PCIe link using a PCIe switch, contact the factory for availability), as well as sideband signals for control and status. Protocols such as Serial Rapid IO and Aurora may be implemented for host communications or custom protocols.

Note that the high speed GTY IO lanes require a host card electrically capable of supporting the high speed signal pairs. Only the eight lane adapter, P/N 80295 is suitable for high speed P16 applications, until release of the new XMC carrier which connects the 8 lane XU-TX links to the 16-lane carrier PCIe link using a PCIe switch, contact the factory for availability).

PCIe-XMC Adapter (80341) x8 PXIe to XMC Clock and trigger inputs	**PCIe-XMC Adapter x8 lane (80295)** x8 PCIe to XMC x8 RIO ports supported on P16	**PCI-XMC Adapter (80167)** 64-bit, 133 MHz PCI-X host x4 PCIe to XMC	**Compact PCI-XMC Adapter (80207)** 64-bit, 133 MHz PCI-X host x4 PCIe to XMC PXI triggers and clock support
			

Applications that need remote or portable IO can use either the eInstrument PC or eInstrument Node with X3 modules.

XU-TX

eInstrument PC with Dual PCI Express XMC Modules (90602) Windows/Linux embedded PC 8x USB, GbE, cable PCIe, VGA High speed x8 interconnect between modules GPS disciplined, programmable sample clocks and triggers to XMCs 2000 MB/s, 4 TB datalogger 9-18V operation	**eInstrument DAQ Node – Remote IO using cabled PCI Express** **(90181)** **Compatible with Notebook or Desktop Host** PCI Express system expansion Up to 10 meter cable Electrically isolated from host computer Software transparent Supports standalone operation of XU modules
	

XU-TX

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